1. A method of establishing a non-transient voltage contrast between a first doped region and a second doped region in a semiconductor wafer portion, said semiconductor wafer portion having a first surface and a second surface opposite said first surface;

said wafer portion having a first semiconductor surface region of said second surface directly atop said first doped region, and having a second semiconductor surface region of said second surface directly atop said second doped region, said voltage contrast being observable on a charged particle beam image of said wafer portion, the method comprising the steps of:

installing said wafer portion in a vacuum chamber in a charged particle beam apparatus;

etching said first semiconductor surface region and said second semiconductor surface region with an etch chemistry for a first time period, for removing an implanted material-containing portion of said first semiconductor surface region and said second semiconductor surface region;

following said first time period, depositing an insulator layer atop said etched first semiconductor surface region and said etched second semiconductor surface region; and

forming an image of said first doped region and said second doped region from secondary electrons emitted from said first and said second doped region, said first doped region being unbiased electrically from said second doped region.

2. The method of claim 1, wherein said step of forming an image utilizes said charged particle beam.

3. The method of claim 1, wherein said charged particle beam is a Focused Ion Beam (FIB).

4. The method of claim 3, wherein said FIB beam is a gallium ion beam.

5. The method of claim 1, wherein said etch chemistry comprises $XeF_2$.

6. The method of claim 1, further including the step of ion milling a deep trench with the charged particle beam prior to the step of etching said first semiconductor surface region and said second semiconductor surface region with an etch chemistry for a first time period.

7. The method of claim 6, wherein said charged particle beam is a Focused Ion Beam (FIB).

8. The method of claim 7, wherein the step of ion milling a deep trench with the focused ion beam comprises milling until a contrast between said first and second doped regions is seen on said image.

9. The method of claim 8, wherein:

said first doped region is a well region having a front surface at said first semiconductor wafer portion surface, and said step of milling until a contrast between said first and second doped regions is seen comprises milling until well contrast is encountered.

10. The method of claim 9, wherein:

the step of ion milling a deep trench with the focused ion beam comprises milling to within 2 - 4 micrometers of said front surface of said well region.

11. The method of claim 8, wherein the step of milling until a contrast between said first and second doped regions is seen on said image includes;

milling at a first beam energy to about 10 microns from said doped regions;

lowering said first beam energy to a second beam energy; and

continuing said ion milling until said contrast is seen between said first doped region and said second doped region on an image.

12. The method of claim 11, wherein said second beam energy is in the range between 10 and 15 KeV.

13. The method of claim 7, wherein said ion milling of a deep trench with the focused ion beam includes utilizing an etch assist chemistry to assist the milling.

14. The method of claim 13, wherein said etch assist chemistry comprises XeF2.

15. The method of claim 14, wherein said XeF2 is flowed at a first flow rate during said ion milling step to maintain a first partial chamber pressure of XeF2, and said step of etching said first semiconductor surface region and said second semiconductor surface region with an etch chemistry for a first time period, for removing an implanted material-containing portion of said

first semiconductor surface region and said second semiconductor surface region comprises:

continuing said flowing of said XeF2 at a second flow rate to maintain a second partial chamber pressure of XeF2 for a second time period while discontinuing said ion milling with said Focused Ion Beam; then

discontinuing said flowing of said XeF2.

16. The method of claim 15, wherein said Focused Ion Beam is a gallium ion beam, said implanted material is implanted gallium from said gallium ion beam, and said second time period of flowing of said XeF2 while discontinuing said ion milling with said Focused Ion Beam is determined to be at least sufficient to provide substantially complete removal of said implanted Ga from said gallium ion beam.

17. The method of claim 16, wherein said second partial chamber pressure of XeF2 is in the range between 2 and 5 x 10-5 Torr, and said second time period is in the range between 3 and 15 seconds.

18. The method of claim 17, wherein said second time period is in the range between 8 and 15 seconds.

19. The method of claim 17, wherein said second partial chamber pressure of XeF2 is about 2.8 x 10-5 Torr, and said second time period is about 10 seconds.

20. The method of claim 1, wherein said insulator layer comprises silicon oxide.

21. The method of claim 20, wherein said silicon oxide is deposited in situ by said FIB beam.

22. The method of claim 21, wherein said depositing of said silicon oxide by said FIB beam includes:

flowing an oxygen- and silicon- containing silicon oxide precursor so as to provide a partial pressure of said oxygen- and silicon- containing silicon oxide precursor in said vacuum chamber for a third period of time while said FIB beam is incident on said wafer portion, said third period of time chosen to yield the desired silicon oxide thickness; then

discontinuing said flowing of said oxygen- and silicon- containing silicon oxide precursor.

23. The method of claim 22, wherein said silicon oxide precursor is selected from the list consisting of: Di-Butoxy-Di-Acetoxy-Silane (DBDAS), Tetraethoxysilane (TEOS), Tetramethylcyclotetrasiloxane (TMCTS), Octamethylcyclotetrasiloxane (OMCTS), Pentamethylcyclopentasiloxane (PMCPS), Dodecamethylcyclopentasiloxane (DMPS), and Tetrakis(dimethylsiloxy)silane (TDMSS).

24. The method of claim 23, wherein said silicon oxide precursor is DBDAS.

25. The method of claim 24, wherein said partial pressure of said DBDAS is about 2.5 x 10-5 Torr, maintained for about 35 min at approximately room temperature.

26. The method of claim 20, wherein said oxide is deposited to a thickness in the range between 100 and 150 nm.

27. The method of claim 20, wherein said oxide is deposited to a thickness in the range between 60 nm and 1 micron.

28. The method of claim 26, wherein said oxide is deposited by said FIB beam having a beam current density in the range between 0.02 and 0.2 $pA/um^2$ , and having a beam energy in the range between 5 and 15 keV.

29. The method of claim 28, wherein said FIB beam has a beam current of about 4nA, and a beam energy of about 15 keV.

30. The method of claim 20, wherein said step of depositing said silicon oxide layer is performed ex situ and includes the steps of:

prior to said depositing of said silicon oxide layer, removing said wafer portion from said charged particle beam system and installing said wafer portion in an oxide deposition system;

depositing said silicon oxide layer onto said wafer portion; and

removing said wafer portion from said oxide deposition system and re-installing said wafer portion into said charged particle beam system.

31. The method of claim 30, wherein said step of depositing said silicon oxide layer onto said wafer portion is performed by a technique selected from the group consisting of: Low Temperature Physical Vapor Deposition (LTPVD), Chemical Vapor Deposition (CVD), and spin-on.

32. The method of claim 31, wherein said oxide is deposited to a thickness in the range between 120 and 140 nm.

33. The method of claim 1, further including exposing said wafer portion to at least one of the group consisting of heat and UV light following insulator deposition to enhance said voltage contrast.

34. The method of claim 33, wherein said exposing includes both heat and UV light.

35. The method of claim 33, wherein said exposing said wafer portion to at least one of the group consisting of heat and UV light includes exposure to heat from a heat source.

36. The method of claim 35, wherein said heat source heats said wafer portion to about 80C for a time period in the range between 5 minutes and 5 hours.

37. The method of claim 33, wherein said exposing to UV light includes exposing said wafer portion to a high power broadband light source.

38. The method of claim 37, wherein said high power broadband light source illuminates said wafer portion for a time period in the range between 5 minutes and 5 hours.

39. The method of claim 1, further including the step of illuminating said wafer portion during insulator deposition.

40. The method of claim 39, wherein said illuminating comprises illumination selected from the group consisting of: IR, visible, and UV wavelengths.

41. The method of claim 40, wherein said illuminating comprises IR illumination operating simultaneously with said charged particle beam.

42. The method of claim 41, wherein said illuminating comprises illumination during in-situ FIB oxide deposition at wavelength centered at 1 um.

43. The method of claim 39, wherein said illuminating lowers the resistivity of said insulator.

44. A method for endpointing the formation of a charged particle beam milled trench in a semiconductor wafer portion having a doped region therein and having a remaining region not coincident with said doped region, said doped region and said remaining region being unbiased electrically from one another, said doped region having a top surface, said trench having a bottom trench surface, comprising the steps of:

milling said trench into said wafer portion at a first particle beam energy and a first particle beam current for a first milling time portion, said bottom trench surface after said first milling time portion being approximately 10 microns separated from said top surface of said doped

region, a first portion of said trench being directly atop at least a portion of said doped region, a second portion of said trench being directly atop at least a portion of said remaining region ;

milling said trench into said wafer portion at a second particle beam energy and a second particle beam current for a second milling time portion while visually monitoring charged particle beam-induced secondary emission levels across said wafer portion, said second particle beam energy being substantially lower than said first particle beam energy; and

halting said milling when a contrast in secondary emission levels between said doped region and said remaining region becomes noticeable.

45. The method of claim 44, wherein said charged particle beam is a Focused Ion Beam (FIB).

46. The method of claim 45, wherein said FIB is a gallium ion beam.

47. The method of claim 46, wherein said second particle beam current is in the range between 0.4nA to 50nA, and said second particle beam energy is in the range between 10 and 15 KeV.

48. The method of claim 47, wherein said second particle beam current is in the range between 2nA to 10nA, and said second particle beam energy is in the range between 10 and 15 KeV.

49. The method of claim 48, wherein said second particle beam current is in the range between 4nA to 10nA.

50. The method of claim 49, wherein said second particle beam current is 4 nA and said second particle beam energy is 15 keV.

51. A method of backside accessing of a specified location on an integrated circuit wafer portion containing a first doped region and a second doped region abutting said doped region comprising the steps of:

ion milling a trench through the backside of said integrated circuit wafer portion with a Focused Ion Beam (FIB) having a first beam energy, to about 10 microns distance from said first doped region;

lowering said first beam energy to a second beam energy and continuing said ion milling until a contrast is seen between said first doped region and said remaining region on an image formed from secondary electrons emitted from said first doped region and said remaining region;

establishing a non-transient voltage contrast between said first doped region and said second doped region using the method of claim 1; and

navigating to said specified location using said image.

52. The method of claim 51, further including performing a modification at said specified location.

53. The method of claim 52, wherein said modification is a circuit edit.

54. The method of claim 51, further including probing said wafer portion at said specified location.

55. The method of claim 54, wherein said probing includes making a measurement.

56. The method of claim 51, wherein said second beam energy is in the range between 10 and 15 KeV.

57. A method of aligning a voltage contrast (VC) FIB image of an integrated circuit wafer portion having corners to a corresponding Computer-Aided Design (CAD) layout so as to probe a target location on said wafer portion, said target location corresponding to a probe location on said CAD layout, said FIB image being produced by a FIB beam having a beam energy and a beam current, said FIB image having a Field of View, said FIB beam being controlled by a computing device including software, comprising the steps of:

performing CAD-IDS OptiFIB 3-point alignment using said corners of said wafer portion;

locally aligning said VC FIB image to said CAD layout by observing said voltage contrast at a FIB beam current in the range between 250 pA and 4 nA;

placing said target location in the center of said Field of View;

forming a spot mark at the exact center of said wafer portion by directing said FIB beam at said center with no dynamic deflection for a period of time approximately equal to 100ms;

lowering said FIB beam current; and

configuring said software to direct said FIB beam at said target location according to said local alignment.

58. A method for determining the vertical cross sectional profile of a doped region in a semiconductor wafer portion, said doped region having a

top surface, said semiconductor wafer portion additionally having a remaining region abutting said doped region, comprising the steps of:

a) forming a trench in said wafer portion by milling with a charged particle beam in a charged particle beam system including a vacuum chamber and having said wafer portion mounted therein, said trench having a bottom surface which encompasses said doped region in at least one horizontal dimension, said trench additionally having side surfaces substantially perpendicular to said bottom surface, said side surfaces being substantially vertical, at least one of said trench side surfaces encompassing said vertical cross sectional profile of said doped region, said trench having a vertical dimension and a lateral dimension, said lateral dimension being in the range between one and three times said vertical dimension;

b) vertically milling said trench all the way through said doped region;

c) depositing a silicon oxide layer onto said wafer portion with a charged particle beam by a method which comprises:

flowing an oxygen- and silicon- containing silicon oxide precursor so as to provide a partial pressure of said oxygen- and silicon- containing silicon oxide precursor in said vacuum chamber for a period of time while said charge particle beam is incident on said wafer portion; then

discontinuing said flowing of said oxygen- and silicon- containing silicon oxide precursor;

d) imaging from said at least one of said trench side surfaces secondary emission from said charged particle beam to form a voltage contrast image between said doped region and said remaining region of said wafer portion, thereby forming a voltage contrast image of said vertical cross sectional profile of said doped region.

59. The method of claim 58, wherein said step of imaging from said at least one of said trench side surfaces includes tilting said wafer portion with respect to said charged particle beam such that said charged particle beam is incident on said at least one of said trench side surfaces.

60. A method for determining the vertical cross sectional profile of a doped region in a semiconductor wafer portion having a horizontal surface, said doped region having a top surface, said semiconductor wafer portion additionally having a remaining region abutting said doped region, comprising the steps of:

a) forming a trench in a cross section of said wafer portion by milling with a charged particle beam in a charged particle beam system including a vacuum chamber and having said wafer portion mounted therein, said trench having a bottom surface which encompasses said vertical cross sectional profile of said doped region;

b) milling said trench parallel to horizontal surface of said wafer until said bottom trench surface reaches said doped region

c) depositing a silicon oxide layer onto said wafer portion with a charged particle beam by a method which comprises:

flowing an oxygen- and silicon- containing silicon oxide precursor so as to provide a partial pressure of said oxygen- and silicon- containing silicon oxide precursor in said vacuum chamber for a third period of time while said charge particle beam is incident on said wafer portion; then

discontinuing said flowing of said oxygen- and silicon- containing silicon oxide precursor; and

d) imaging secondary emission from said bottom trench surface with said charged particle beam to form a voltage contrast image across both said cross section of said doped region and said remaining region of said wafer cross section portion;

61. A method for determining the vertical profile of a doped region in a semiconductor wafer portion, said doped region having a top surface, said semiconductor wafer portion additionally having a remaining region abutting said doped region, comprising the steps of:

a) forming a trench in said wafer portion by milling with a charged particle beam in a charged particle beam system including a vacuum chamber and having said wafer portion mounted therein, said trench having a bottom surface which encompasses said doped region;

b) vertically milling said trench until said bottom trench surface reaches said top surface of said doped region;

c) depositing a silicon oxide layer onto said wafer portion with a charged particle beam by a method which comprises:

flowing an oxygen- and silicon- containing silicon oxide precursor so as to provide a partial pressure of said oxygen- and silicon- containing silicon oxide precursor in said vacuum chamber for a third period of time while said charge particle beam is incident on said wafer portion; then

discontinuing said flowing of said oxygen- and silicon- containing silicon oxide precursor;

d) imaging secondary emission from said bottom trench surface with said charged particle beam to form a voltage contrast image between said doped region and said remaining region of said wafer portion;

e) milling an additional vertical increment; then

f) repeating steps c), d), and e) until said trench is milled all the way through the doped region.

62. The method of claim 61, wherein said charged particle beam is a FIB beam having a beam current density in the range between 0.02 and 0.2 $pA/um^2$ , and having a beam energy in the range between 5 and 15 keV.

63. The method of claim 60, wherein said charged particle beam is a FIB beam having a beam current density in the range between 0.02 and 0.2 $pA/um^2$ , and having a beam energy in the range between 5 and 15 keV.

64. The method of claim 58, wherein said charged particle beam is a FIB beam having a beam current density in the range between 0.02 and 0.2 $pA/um^2$ , and having a beam energy in the range between 5 and 15 keV.

65. The method of claim 58, further comprising just before the step of depositing a silicon oxide layer onto said wafer portion:
flowing XeF2 at a flow rate to maintain a partial pressure in the range between 2 and 5 x 10-5 Torr of XeF2 in said vacuum chamber for a time period in the range between 3 and 15 seconds while discontinuing said milling with said FIB; then

discontinuing said flowing of said XeF2.

66. The method of claim 60, further comprising just before the step of depositing a silicon oxide layer onto said wafer portion:

flowing XeF2 at a flow rate to maintain a partial pressure in the range between 2 and 5 x 10-5 Torr of XeF2 in said vacuum chamber for a time period in the range between 3 and 15 seconds while discontinuing said milling with said FIB; then

discontinuing said flowing of said XeF2.

67. The method of claim 61, further comprising just before each step of depositing a silicon oxide layer onto said wafer portion:
flowing XeF2 at a flow rate to maintain a partial pressure in the range between 2 and 5 x 10-5 Torr of XeF2 in said vacuum chamber for a time period in the range between 3 and 15 seconds while discontinuing said milling with said FIB; then

discontinuing said flowing of said XeF2.

68. An integrated circuit intermediate product, comprising:

a semiconductor wafer portion having a doped region therein at a surface thereof, and further having a remaining region abutting said doped region at said surface;

said semiconductor wafer portion surface having a silicon oxide layer thereon with a thickness in the range between 100 and 150 nm;

said semiconductor wafer portion showing a non-transient voltage contrast between said doped region and said remaining region when imaged by secondary emission induced by a charged particle beam incident on said wafer portion.

69. The integrated circuit intermediate product of claim 68, fabricated by the method of claim 26.

70. A system comprising:

a charged particle beam column for generating a charged particle beam that, when directed at a location on a surface of an integrated circuit wafer portion, generates secondary electrons;

a detector for detecting said secondary electrons;

an image generator for generating, based on an output of said detector, an image of structures underlying said surface of said wafer portion;

a computing device configured to navigate, based on said image, to a specified location on said wafer portion; and

a source of at least one of: light and heat, for exposing said wafer portion thereto in situ.

71. The system of claim 70 wherein said charged particle beam column is a focused ion beam column.

72. The system of claim 70 wherein said detector is a scintillator.

73. The system of claim 70 wherein said source of at least one of: light and heat includes a UV source.

74. The system of claim 70 wherein said image is a voltage contrast image.

75. A method of observing voltage contrast from buried structures under a surface of a Silicon On Insulator (SOI) structure having exposed oxide comprising the steps of:

depositing a Pt layer of thickness less than 5 nm on said SOI structure; and

etching said Pt layer with Ethylene Di-Iodide (EDI) to remove said Pt layer at differing rates according to surface potential induced by said buried structures.

76. The method of claim 75, further including the step of aligning said SOI structure to a corresponding CAD according to said observed voltage contrast.